polarizone

MSC-Status Company

2 in 2 out MIMO DESIGN BENCH SPECIFICATION

Applications

- Study of MIMO systems.
- 2 in 2 out MIMO system design and performance analysis.
- Space time block and trellis code design, real time implementation and performance verification.
- Channel estimation and and MIMO synchronization, MIMO receiver algorithms design and real time implementation.
- High performance MIMO wireless system prototyping.
- Real time implementation of transmit and receive subsystems.
- Direct Digital Synthesis (DDS), Digital Up-Conversion (DUC).
- Built in power supplies & RF sources.
- RF frequency and power selection.

Hardware

- MIMO Transmitter.
- MIMO Receiver.
- USB to JTAG programming cable - 2 Nos
- Patch antenna - 4 Nos, Cables

Features

- FPGA's – 2 numbers of Virtex-4. One each for transmission and reception.
- DSP processor – 2 numbers of TIDSP
- High Speed ADC/DAC cards - 1 number of #
- Memory – 128M x 32 connected to each TIDSP on EMIFA interface
- Boot prom(s) for DSP processor(s) and their programming interface using JTAG.

Technical Specifications for 2 in 2 out MIMO Design Bench

****Virtex-4 (Platform: LX, SX, FX) + TIDSP + ARM Processor**

- LX: High performance logic.
- SX: Ultra high performance signal processing.
- FX: Embedded processing and serial connectivity.

#Analog Module

- Two (2) 14 bits 125 MSPS A/D converters
- Single ended 50 ohm inputs.
- Low pass 7th order RLC anti-alias filter.
- Two (2) 16 bits 500 MSPS D/A converters.
- Transformer coupled 50 ohm outputs.
- Low pass 5th order RLC reconstruction filter.

RF Transceiver

- 2.4GHz to 2.5GHz ISM Band operation.
- 802.11a/b/g PHY compatible.
- Integrated PA power detector.
- Integrated Transmit/Receive Switch.
- Complete RF to Baseband Transceiver
  - Direct up/down conversion
  - Monolithic low phase nosie VCO
  - Integrated Baseband LPF
  - Integrated PLL with 3 wire serial interface
  - Digital bias control for power Amplifier
  - Transmit power control
  - Complete Baseband interface
- 75 dbm receiver sensitivity at 54 MBPS (802.11g).
- Single +2.7V to +3.6V power supply.

Note:
The institution should provide Original Xilinx ISE foundation and Chipscope pro for compiling all VHDL library files and viewing all FPGA signals like ADC input.

*** Ask for Separate Quotation for difference platform of Virtex-4 series, and add-on of TIDSP and ARM Processor.*

Basic unit cost:

www.polarizone.com

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